Course Code: 16EC431

R16

SIDDHARTH GROUP OF INSTITUTIONS:: PUTTUR
(AUTONOMOUS)
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QUESTION BANK (DESCRIPTIVE)

Subject with Code: VLSI Dessign (16EC431) **Course & Branch**: B.Tech - ECE

Year & Sem: IV-B.Tech & I-Sem **Regulation:** R16

UNIT –I
INTRODUCTION

1	a) Explain the steps involved in fabrication of a p-well process CMOS transistor.	[L2][CO1]	**[7M]**
	b) List steps involved in n-well process.	[L1][CO1]	**[5M]**
2	a) Explain clearly about Moore's law.	[L2][CO1]	**[4M]**
	b) Explain the different steps in n-well fabrication of CMOS transistor, with neat diagrams.	[L5][CO1]	**[8M]**
3	a) What is the need of VLSI circuits?	[L1][CO1]	**[5M]**
	b) Compare the relative merits of three different forms of alternative pull ups for an inverter circuit.	[L1][CO1]	**[7M]**
4	a) Compare CMOS with Bipolar transistors in different aspects.	[L4] [CO1]	**[6M]**
	b) Design the circuit diagram of a simple BiCMOS inverter and explain its operation.	[L6][CO1]	**[6M]**
5	Determine the relationship between I_{ds} & V_{ds} in non-saturated and saturated region.	[L4][CO1]	**[12M]**
6	Explain the n-MOS fabrication steps with neat sketches and use p^+ masking.	[L5][CO1]	**[12M]**
7	a) Discuss the MOS Transistor operation of three conditions with the help of neat sketches	[L6][CO1]	**[6M]**
	b) Illustrate the operation of Bi-CMOS inverter and draw the different alternative structures.	[L3][CO1]	**[6M]**
8	Discuss the following.	[L6][CO1]	**[12M]**
	a) Transconductance ($g_{m)}$ and output conductance (g_{ds}).		
	b) Figure of merit (ω_o).		
9	a) Defend why NMOS technology is preferred more than PMOS technology.	[L5][CO1]	**[4M]**
	b) Discuss the generations of Integrated Circuits.	[L6][CO1]	**[8M]**
10	Analyze the different types of alternative pull-ups with neat sketches.	[L4][CO1]	**[12M]**

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UNIT –II
VLSI CIRCUIT DESIGN PROCESS

1	a) Explain the different steps involved VLSI Design flow.	[L2][CO2]	**[6M]**
	b) What is a stick diagram? Design the stick diagram of a three input CMOS NAND gate.	[L1&L6][CO2]	**[6M]**
2	a) Discuss the lambda-based design rules with neat sketches.	[L6][CO2]	**[6M]**
	b) Explain design rules for wires and MOS transistors.	[L6][CO2]	**[6M]**
3	a) Explain 2µm based design rules with neat sketches.	[L6][CO2]	**[6M]**
	b) Build a stick diagram and layout of NMOS inverter circuit. Both Input and Output points should be Polysilicon layer.	[L6][CO2]	**[6M]**
4	a) Explain about Stick's diagram with suitable examples.	[L2][CO2]	**[6M]**
	b) Develop the schematic and layout for 2-input NAND gate	[L6][CO2]	**[6M]**
5	a) Design the stick diagram for CMOS inverter?	[L6][CO2]	**[5M]**
	b) Design the layout diagram for CMOS inverter?	[L6][CO2]	**[7M]**
6	a) Create a stick diagram for Y= (AB+CD)' using NMOS design style.	[L6][CO2]	**[6M]**
	b) Design the schematic and layout diagram of 2-input NOR gate using CMOS deign style.	[L6][CO2]	**[6M]**
7	Plan and design a layout diagram for the following functions in CMOS logic.	[L6][CO2]	**[12M]**
	y= [(a+b).c]'.		
	z= (ab+cd+e)'		
8	a) Organize the layers how polysilicon and Metal type1 contact cut are happen.	[L3][CO2]	**[5M]**
	b) Explain how the p-MOS transistor forms in lambda-based design rules.	[L2][CO2]	**[7M]**
9	a) Build the layout of AND-OR-INVERTER in NMOS design Styles.	[L6][CO2]	**[8M]**
	b) Demonstrate how implant and demarcation lines employed in stick diagrams.	[L3][CO2]	**[4M]**
10	a) What is MOS layer?	[L1][CO2]	**[4M]**
	b) Explain different types of MOS layers used in VLSI circuits.	[L3][CO2]	**[8M]**

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UNIT –III
GATE LEVEL DRSIGN & PHYSICAL DESIGN

1	a) Design the CMOS implementation of 2X1 mux using transmission gates.	[L6][CO3]	**[5M]**
	b) Explain the AOI implementation using CMOS design style with neat sketches.	[L2][CO3]	**[7M]**
2	a) What is switch logic?	[L2][CO3]	**[4M]**
	b) Explain about pass transistors and transmission gate.	[L1][CO3]	**[8M]**
3	a) What is pseudo NMOS logic?	[L1][CO3]	**[4M]**
	b) Design the 2 input NAND gate by using pseudo NMOS logic.	[L6][CO3]	**[8M]**
4	a) Illustrate the dynamic CMOS logic circuit with any one example.	[L2][CO3]	**[8M]**
	b) List advantages & disadvantages of dynamic CMOS logic	[L1][CO3]	**[4M]**
5	Discuss the following below	[L6][CO3]	**[12M]**
	a) Domino CMOS logic.		
	b) NORA logic.		
6	Explain about complex logic gates with examples.	[L2][CO3]	**[12M]**
7	What is the necessity of floor planning concept in VLSI circuits? and discuss with suitable example.	[L1&L6][CO3]	**[12M]**
8	What are the design methods used in physical design cycle? Explain the each term with suitable diagrams.	[L1&L2][CO3]	**[12M]**
9	a) Explain how the clock and power distributions employed in VLSI design circuits with diagrams.	[L2][CO3]	**[6M]**
	b) Illustrate the Power delay estimation in VLSI circuits.	[L2][CO3]	**[6M]**
10	Explain and elaborate the following below	[L2&L6][CO3]	**[12M]**
	a) Floorplanning		
	b) Placement		
	c) Routing		

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UNIT –IV
SUB SYSTEM DESIGN

1	Explain the design of different adders in sub circuit design with neat sketches.	[L1&L6][CO4]	**[12M]**
2	a) What is shifter? List the types of shit registers.	[L1][CO4]	**[6M]**
	b) Design and explain the shifter implemented by using full adder.	[L6&L2][CO4][5M]	**[6M]**
3	Extend the following sub circuits	[L2][CO4]	**[12M]**
	a) Parity generators		
	b) Comparators		
4	Design a Arithmetic and Logic Unit circuit with four functions by using multiplexer logic.	[L6][CO4]	**[12M]**
5	a) Explain about different types of memory elements.	[L2][CO4]	**[6M]**
	b) Construct the 4*4 array multiplier	[L3][CO4]	**[6M]**
6	Explain the working of Zero/one detector implemented with adder circuit.	[L2][CO4]	**[12M]**
7	Demonstrate the following	[L2][CO4]	
	a) Unsigned magnitude comparator		**[6M]**
	b) Asynchronous Counters		**[6M]**
8	a) Design and Explain the circuit diagram of 3-bit LFSR with example.	[L6&L2][CO4]	**[6M]**
	b) Design and Explain the Johnson counter.	[L6&L2][CO4]	**[6M]**
9	a) Design and Explain the circuit diagram of four bit Carry ripple adder.	[L6&L2][CO4]	**[6M]**
	b) Design and Explain the the ripple counter.	[L2][CO4]	**[6M]**
10	a) Explain about 4 transistor Dynamic memory cell.	[L2][CO4]	**[6M]**
	b) Explain the 6 transistor Static memory cell.	[L2][CO4]	**[6M]**

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UNIT –V
SEMICONDUCTOR INTEGRATED CIRCUIT DESIGN AND CMOS TESTING

1	a) Compare the PROM,PAL, PLA.	[L2][CO5]	**[6M]**
	b) Design the PAL Structure for the Boolean function Y= AB'C'+ABC+A'B'C'+A'BC.	[L6][CO5]	**[6M]**
2	a) Design and explain the architecture of FPGA.	[L6][CO5]	**[6M]**
	b) Discuss the merits of FPGA over other architectures.	[L6][CO5]	**[6M]**
3	a) Discuss in details about CPLD structure and explain each block.	[L6][CO5]	**[6M]**
	b) What is global routing? Discuss the advantages.	[L1&L6][CO5]	**[6M]**
4	Design the logic diagram of PLA for the following. Y1=A'B'C'+ABC+A'B+ABC' Y2=ABC+A'B'C+AC Y3=A'BC'+AB'C+B'C'	[L6][CO5]	**[12M]**
5	a) Discuss in detail about standard cell design with suitable diagrams.	[L6][CO5]	**[6M]**
	b) Demonstrate the following i) I/O pads ii) SPLD iii) LUT	[L2][CO5]	**[6M]**
6	a) What is the need for testing? and explain about Fault simulation.	[L1&L2][CO5]	**[6M]**
	b) Discuss the necessity of testing VLSI circuits.	[L6][CO5]	**[6M]**
7	a) Explain about design strategies for testing.	[L2][CO5]	**[6M]**
	b) Construct With neat sketches list the testing of various stages.	[L3][CO5]	**[6M]**
8	Explain in detail about testing during the VLSI life cycle with neat sketches.	[L2][CO5]	**[12M]**
9	a) What is testing? And explain any three test principles.	[L1&L2][CO5]	**[6M]**
	b) What is controllability and observability?	[L1][CO5]	**[6M]**
10	a)What is fault simulation?	[L1][CO5]	**[4M]**
	b) Explain the stuck at 1 and stuck 0 faults with suitable diagrams.	L2][CO5]	**[8M]**

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